along with any additional mechanical design or data (if applicable), to generate a second design structure **120**. Design structure **120** resides on a storage medium or programmable gate array in a data format used for the exchange of data of mechanical devices and structures (e.g. information stored in an IGES, DXF, Parasolid XT, JT, DRG, or any other suitable format for storing or rendering such mechanical design structures). Similar to design structure **102**, design structure **120** preferably comprises one or more files, data structures, or other computer-encoded data or instructions that reside on transmission or data storage media and that when processed by an ECAD system generate a logically or otherwise functionally equivalent form of one or more of the embodiments of the invention shown in FIG. **9** and FIG. **12**. In one embodiment, design structure **120** may comprise a compiled, executable HDL simulation model that functionally simulates the devices shown in FIG. **9** and FIG. **12**.

Design structure **120** may also employ a data format used for the exchange of layout data of integrated circuits and/or symbolic data format (e.g. information stored in a GDSII (GDS2), GL1, OASIS, map files, or any other suitable format for storing such design data structures). Design structure **120** may comprise information such as, for example, symbolic data, map files, test data files, design content files, manufacturing data, layout parameters, wires, levels of metal, vias, shapes, data for routing through the manufacturing line, and any other data required by a manufacturer or other designer/developer to produce a device or structure as described above and shown in FIG. **9** and FIG. **12**. Design structure **120** may then proceed to a stage **122** where, for example, design structure **120**: proceeds to tape-out, is released to manufacturing, is released to a mask house, is sent to another design house, is sent back to the customer, etc.

The method as described above is used in the fabrication of integrated circuit chips. The resulting integrated circuit chips can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case, the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

It will be understood that when an element is described as being "connected" or "coupled" to or with another element, it can be directly connected or coupled to the other element or, instead, one or more intervening elements may be present. In contrast, when an element is described as being "directly connected" or "directly coupled" to another element, there are no intervening elements present. When an element is described as being "indirectly connected" or "indirectly coupled" to another element, there is at least one intervening element present.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The embodiment was chosen and described in order to best explain the principles of the invention and the practical application, and to enable others of ordinary skill in the art to understand the invention for various embodiments with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A device structure for a bipolar junction transistor, the device structure comprising:
- an intrinsic base including a top surface;
- an extrinsic base on the top surface of the intrinsic base;
- a silicide layer on the extrinsic base;
- a plurality of first spacers having an outer surface, the first spacers oriented to project vertically relative to the top surface of the intrinsic base, the first spacers arranged to line an emitter window therebetween, and the emitter window extending through extrinsic base and the silicide layer to the top surface of the intrinsic base; and
- an emitter including a portion disposed in the emitter window and a head protruding out of the emitter window, the portion of the emitter in contact with the intrinsic base, and the portion of the emitter having a plurality of sidewalls that border the first spacers and that are separated from the extrinsic base and the silicide layer by the first spacers,
- wherein the silicide layer and the extrinsic base each terminate at the outer surface of the first spacers so that the silicide layer and the extrinsic base are aligned relative to each other and relative to the portion of the emitter by the first spacers.

2. The device structure of claim **1** wherein the silicide layer comprises titanium (Ti), cobalt (Co), or nickel (Ni).

3. The device structure of claim **2** wherein the silicide layer comprises semiconductor material from the extrinsic base.

4. The device structure of claim **1** further comprising:
- an insulating layer on the silicide layer, the insulating layer separated from the extrinsic base by the silicide layer.

5. The device structure of claim **1** wherein the extrinsic base directly contacts the top surface of the intrinsic base, and the extrinsic base has an epitaxial relationship with the intrinsic base.

6. The device structure of claim **1** further comprising:
- a plurality of second spacers lining the emitter window, the second spacers disposed between the emitter and the first spacers.

7. The device structure of claim **1** further comprising:
- a plurality of trench isolation regions in a semiconductor substrate that surround a device region; and
- a collector region in the device region, the collector region coupled with the raised region of the intrinsic base and separated from the emitter by the intrinsic base.